INDIAN INSTITUTE OF MANAGEMENT CALCUTTA

WORKING PAPER SERIES

WPS No. 661/ August 2010

A Novel Approach for Solving Multi-objective Optimization Problems: A Case of VLSI Thermal Placement

by

Ram Babu Roy
Doctoral student, IIM Calcutta, Joka, Diamond Harbour Road, Kolkata 700104, India

Debashis Saha
Professor, IIM Calcutta, Joka, Diamond Harbour Road, Kolkata 700104, India

&

Parthasarathi Dasgupta
Professor, IIM Calcutta, Joka, Diamond Harbour Road, Kolkata 700104, India

A Novel Approach for Solving Multi-objective Optimization Problems: A Case of VLSI Thermal Placement

Ram Babu Roy*, Debashis Saha and Parthasarathi Dasgupta

Abstract—We often confront with optimization problems that require optimizing multiple objectives. Such multi-objective optimization problems are often non-linear in nature and are hard to solve. In such situations conventionally heuristic methods are used to arrive at some reasonably good solutions. VLSI standard cell placement problems traditionally have to handle multiple objectives such as area, delay, thermal distribution and so on, to arrive at a reliable design. One of the key concerns in this area is to simultaneously (i) optimize the thermal distribution of the heat dissipated by the logic gates on the chip and (ii) minimize the total wirelength required to interconnect these gates. This in turn helps in reducing the chances of occurrence of hot spots on the chip, on-chip delay and the total chip area. Optimizing these objectives individually is known to be NP-hard and hence simultaneous optimization of the two objectives is a challenging problem. In this work, we have also proposed a game-theoretic formulation to the problem and developed some novel heuristic algorithms for solving this problem. The proposed algorithms have been implemented, and the experimental results are quite encouraging.

***Index Terms*— optimization methods, Integrated Circuit layout design, game theory, heuristic methods**

I. Introduction

Modern business scenario gives us plenty of examples of competition and co-operation as available resources are scarce. On one hand, firms in the market may have to compete with each other on some issues and on the other hand they have to cooperate with each other on some other issues. To survive in the cut throat competition the decision makers need to optimize multiple objectives simultaneously under several constraints and, therefore, they resort to some trade-offs. For designing the retail shop networks for supply chain management, we need to identify optimum locations for warehouses and retail shops so as to maximize the footfall and minimize the total transportation cost. A logistics and transportation company may have to design the pick-up-cum-delivery point networks to reduce delay and cost. Similarly, Electronic Design Automation (EDA) tools for integrated circuit design in the nanometer range have to consider several decision variables and constraints to optimize multiple (often conflicting) objectives. In such situations, we are interested in optimizing multiple objectives simultaneously while satisfying the constraints. In this paper, we discuss a game theoretic approach for the placement of standard cells on a chip layout so as to optimize two key parameters namely the total wirelength and the temperature distribution across the chip. In this paper, we refer standard cell as cell.

*corresponding author
This work was supported in part by a research grant from the Department of Information Technology (DIT), Govt. of India.
Ram Babu Roy is a research student with Management Information Systems Group at the Indian Institute of Management Calcutta, Kolkata-700104, India. phone: +91-9903883394; fax: +91-33-2467-8062; e-mail: rbroy07@iimcal.ac.in).
Debashis Saha and Parthasarathi Dasgupta are professors with Management Information Systems Group at Indian Institute of Management Calcutta, Kolkata-700104. (e-mail: ds@iimcal.ac.in, partha@iimcal.ac.in).

II. Motivation

The total wirelength *L* is a widely used measure of the quality of placement. The area of the layout consists of two parts: the functional area and the wiring area [2]. The total functional area remains the same for all the placements but the wiring area changes with the placement. The total wirelength L is thus a reasonable measure of area of the layout. Reducing the total wirelength can help in reducing the chip area as well as the power dissipation and hence the chip temperature. The placement of cells in order to minimize the total wirelength L is NP-hard [2]. Also, in order to observe the temperature distribution on the chip, generally a temperature window is defined and the temperature of the window is monitored. The placement of the cells in order to minimize the maximum window temperature is also a NP-hard problem [3].

Considering the above two factors, a natural question would be: *Is it possible to obtain a placement of logic cells in a chip having uniformly distributed power dissipation (and hence temperatures), and reasonably small total interconnect length?* Our work attempts to provide an answer to this question through game theoretic modeling and associated heuristic techniques.

III. Literature review

As feature size in a VLSI chip reduces, thermal effect becomes dominant and affects severely the chip performance. Transistor speed is slower at higher temperature due to reduction in carrier mobility. The leakage power increases with chip temperature [1] and the increased leakage power in turn increases the chip temperature reinforcing its severity. The metal resistivity of the interconnecting wire is also dependent on temperature and increases with the increase in temperature. Higher resistivity causes larger interconnect RC delay and higher I^2R heating. Proper distribution of the power dissipation of the logic gates on a chip is crucial for improving circuit performance and reliability. Thus, it is imperative to minimize occurrence of high-temperature regions (hotspots) in a placement of logic cells in a chip.

Several attempts have been made to solve this problem and the results have been widely published in the literature. Chu and Wong have modeled the thermal placement problem as a Matrix Synthesis Problem (MSP) and suggested some nice algorithms to solve it [3]. To observe the variation in temperature on the chip we need some window to observe the temperature at a point. The size of window depends on the rate of heat transfer on the substrate [3]. If the heat transfer is poor the effect is only on the neighbor cell so we may choose a smaller window. If the heat transfer is good the effect is seen on the larger region so we may choose a larger window.

The temperature at a point on the chip is determined by power dissipation of neighboring nodes within a certain distance. The time constant of on-chip heat conduction is in the range of milliseconds, which is orders of magnitudes larger than the clock cycles being used today [7]. As a result, once the thermal steady state is reached, the chip temperature does not follow the instantaneous power dissipation, but instead remains virtually constant. Thus, for full-chip thermal analysis, we are generally concerned with the steady-state case and not the transient analysis. Tsai and Kang [7] have proposed a nice modeling of the problem by transposing the temperature distribution problem into a power distribution problem. The substrate is discretized and modeled as a three-dimensional (3-D) lumped circuit network, and the temperature is found by solving the nodal equation of the network numerically using the Finite Difference (FD) method.

Game theoretic formulation has been applied to solve several problems in economics and other management problems. To the best of our knowledge, not many significant works have been reported so far on the application of Game Theory to VLSI design. Game Theory has recently captured attention of researchers to apply it for solving problems in VLSI domain. Hanchate and Ranganathan have used Game Theory for Simultaneous Optimization of Interconnect Delay and Crosstalk Noise through Gate Sizing [4]. Murugavel and Ranganathan have used a Game-Theoretic Approach for Binding in Behavioural Synthesis [5].

IV. Problem formulation

Matrix Synthesis Problem (MSP) was introduced in [3]. This involves synthesizing a matrix from a given list of numbers representing the amount of heat generated by standard cells such that no sub-matrix (window) of a particular size has a sum larger than some specified limit. The sub-matrix with the largest sum represents the hottest region on the chip. We consider the MSP problem with a matrix of size ($m \times m$), and window size ($t \times t$) and an additional objective of minimizing the total wirelength. We define the following parameters to measure the quality of the placement.

T_{max} = maximum window temperature on the chip
T_{avg} = the average value of the window temperature and
$DeltaT = T_{max} - T_{avg}$ = the maximum deviation of the window temperature from T_{avg}

$WT^k = \sum_{i=1}^{t}\sum_{j=1}^{t} T_{ij}^k$ is the window temperature of the k^{th} window

where T_{ij}^k is the temperature of the i^{th} row and j^{th} column of the k^{th} window. The index k represents the k^{th} window and varies from 1 to $(m/t)^2$. T_{avg} is the window temperature of each window under ideal condition i.e. assuming uniform temperature across the chip. *DeltaT* measures the maximum deviation from this ideal situation and can be considered as a measure of the quality of temperature distribution. We want to simultaneously optimize two objectives (1) minimizing the maximum window temperature T_{max} and (2) minimizing the total wirelength L of all interconnecting nets. While attempting to minimize one objective, the value of other objective function may increase. Therefore, we impose some restriction such that the value of any objective function should not increase beyond its initial (starting point) value. We also want a temperature distribution across the chip such that the maximum deviation of window temperature from the average window temperature is within some permissible limit $DeltaT_{max}$. $DeltaT_{max}$ can be defined as some percentage of T_{avg}. Thus, the problem can be formulated as:

Given the value of m, t and a list of m^2 non-negative integers representing the gate temperature and the adjacency matrix of the gate cells, synthesize a matrix of size (m x m) out of m^2 non-negative integers optimizing the following two objectives.

Objective 1: Minimize $T_{\max} = \underset{k \in [1, (\frac{m}{t})^2]}{\mathrm{maximum}} \ (WT^k)$

Objective 2: Minimize $L = \sum_{\substack{i,j=1 \\ j>i}}^{N} \left\{ \left|R(i) - R(j)\right| + \left|C(i) - C(j)\right| \right\} \ w_{ij}$

where *R(i)* and *C(i)* are the row and column coordinate of the cell *i* as shown in Figure 3 and w_{ij} is the interconnect weight between cell i and cell j as shown in Figure 2.
The constraints to be satisfied are:
$T_{max} < T_{max}(initial)$
$L < Lmax(initial)$
$DeltaT < DeltaT_{max}$

V. MODELING THE MULTI-OBJECTIVE OPTIMIZATION PROBLEM

We have modeled the multi-objective optimization problem as a combinatorial optimization Matrix Synthesis Problem (MSP) similar to what has been discussed in [3]. The matrix has four sets of cells with each set having a different color band say black (B), pink (P), green (G) and red (R) as shown in Figure 1. The connectivity of the cells (gates) is represented by an adjacency matrix as shown in Figure 2.

B	R	B	R	B	R	B	R
G	P	G	P	G	P	G	P
B	R	B	R	B	R	B	R
G	P	G	P	G	P	G	P
B	R	B	R	B	R	B	R
G	P	G	P	G	P	G	P
B	R	B	R	B	R	B	R
G	P	G	P	G	P	G	P

Figure 1: A Scheme for placement of cells of various colors

The coloring of the cells is done based on the temperature of the corresponding gates and hence the color of a cell captures its temperature information. In order to assign colors to the cells of the matrix, we arrange the cells in non-decreasing order of their temperature and partition them into four equal quarters. The cells in the first quarter are assigned black color (these are relatively colder), the cells in the second quarter are assigned pink color and so on with red assigned to the cells in the fourth quarter (i.e. relatively hotter cells). This assignment ensures that the cells with the same color have relatively closer temperature values. In order to distribute the temperature uniformly, we impose a restriction that no two cells of the same color can stay adjacent to each other as shown in Figure 1. This helps in achieving a reasonably uniform temperature distribution on the chip.

The weight of interconnections between the cells can be represented by the adjacency matrix *W*. By weight of interconnections we mean the number of interconnections between the cells. The top-most row (*R*) and the left-most column (*C*) contain the cell numbers that identify the cells. Therefore, an element $w_{ij} \in W$ is fixed by the functionality requirement of the VLSI circuit and captures the information regarding the weight of the interconnection between the cells, so we need to consider only the difference in the rows (*R)* and the columns (*C*) of the displaced cells while changing the topology of the placement during the optimization process. Figure 2 shows a schematic representation of the adjacency matrix with associated interconnect weights. The entry at the intersection of row (i) and column (j) represents the weight of interconnection between two cells represented by the serial number i and j. If $w_{ij} = 0$, it implies that there is no connection between cells *i* and *j*.

	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
0	0	0	1	0	3	0	2	0
1	0	0	0	0	0	6	0	0
2	1	0	0	4	0	0	5	0
3	0	0	4	0	0	0	0	0
4	3	0	0	0	0	0	0	5
5	0	6	0	0	0	0	0	0
6	2	0	5	0	0	0	0	3
7	0	0	0	0	5	0	3	0

Figure 2: Adjacency matrix with associated interconnect weight

Figure 3 shows a diagram for estimating *L* which can be calculated as the weighted sum of the Manhattan distances using the formula given below.

$$L = \sum_{\substack{i,j=1 \\ j>i}}^{N} \left\{ |R(i) - R(j)| + |C(i) - C(j)| \right\} w_{ij}$$

where *R(i)* and *C(i)* respectively represent the row and column coordinates of the cell i.

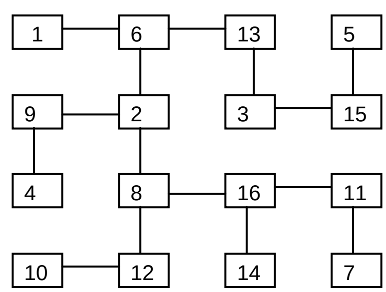


Figure 3: An example diagram showing wirelength

VI. GAME THEORETIC APPROACH

We have attempted a game-theoretic approach to model the multi-objective optimization problem. In order to apply game theory to this problem we need to decide on the following

a) What type of game to choose
b) How to choose the players
c) How to decide the strategies of the players
d) How to compute the payoffs of the players

A. Deciding the type of game

We need to decide on what type of game to play. In this particular problem, we have many players and the payoff of a player depends on the previous actions of all other players.

The aim of the players is to achieve a collective optimum goal even if the actions are not in the best of their private interest. Such many-player games are called *collective-action games*. The socially optimal outcome is not automatically achievable as the Nash equilibrium of the game [6]. We choose two sub-teams sequentially based on connectivity and proximity between the cells. The players of both the teams play in teams and have a common strategy of accepting the moves or rejecting the moves depending on the collective gain of both the teams. The strategy corresponding to a positive payoff is selected. If the pay-off is negative, we reject the move and select new sub-teams.

B. Choosing the players

The choice of players is an important issue as this ensures the uniformity in the temperature distribution across the chip. The rules for choosing the players for simultaneous optimization of temperature distribution and total wirelength are given below.

- After thermal placement using algorithm 1 (discussed in the next section) we obtain approximately uniform thermal distribution and assign colors to all the cells and the T_{max} is very close to the ideal T_{avg}
- Compute the total interconnect weight of each cell and arrange the cells in non-increasing order of their total interconnect weight
- Choose the cell with the highest interconnect weight as the seed cell
- Take the three neighbours of the seed cell from its associated window (t = 2) as players {*p1, p2, p3*} in team 1. Note that these three players will be of three different colors due to the restriction imposed by Algorithm 1 that no two neighbors would have same color
- Take three cells heavily connected with the seed cell and each with three different colors matching with the colors of the players of team 1 as the three players {*p4, p5, p6*} in team 2
- Play the game of swapping positions amongst the players of these two teams so as to minimize the total wire length

C. Deciding the strategies of the players

We consider two teams each comprising three players. In general, a player has three possible strategies of exchanges with players of the other team. The payoff depends on the sequence of moves of the players. So we need to decide the priority in choosing the players for playing the sequential game. For 3 players of one team we have 3 positions of players of other team to exchange their positions. If we assign first preference to player 1, second preference to player 2, and so on, we have the following 6 possible strategies of exchanges given by ${}^{3}P_{3}$ as shown in Figure 4. Player P1 can swap its position with any one of the three players from other team. Subsequently, player P2 can swap its position with remaining two and player P3 can swap with the remaining one player of the other team. We can select the one giving the maximum payoff.

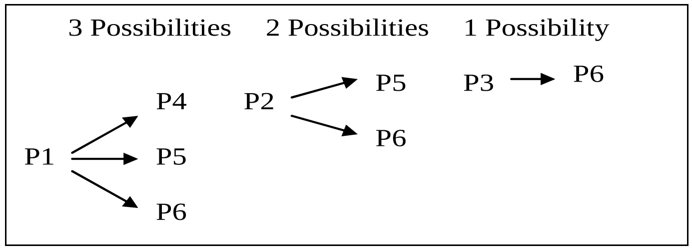


Figure 4: Schematic for possible exchanges between players

D. Computing the payoffs of the players

We can compute a composite payoff as a linear combination of amount of reduction in the total wirelength and the amount of reduction in temperature. The coefficients of the linear combination depend on the priority level for the two objectives of optimization. If we assume that both the objectives have equal priority then we can use proper scaling to determine the value of these coefficients. Since we have classified the cells into four color bands and if we restrict the exchange between the players with the same color i.e. intra-band exchange so that the temperature distribution achieved by algorithm 1 is not disturbed significantly. We can use this restricted exchange here to simplify the payoff function. Therefore, the number of possible exchanges between the two teams of players reduces to a set of three exchanges of positions for the players of same color one from each team. In this situation, we can allow simultaneous move for the players of the two teams and compute the negative of the change in the wirelength *DeltaL* associated with a particular set of moves as a collective payoff for that iteration. Since the temperature distribution has been taken care of by restricting the exchanges with players of same color, we need to optimize our other objective of reducing the total wire length. Any move reducing the total wire length is a favourable move and any move increasing the total wire length is an unfavorable one. Therefore, the teams accept the move giving positive collective payoff after all the three exchanges and reject that with a negative payoff.

VII. Proposed Algorithms

We have proposed two algorithms. Algorithm 1 (shown in Figure 5) is similar to the one proposed in [3] and is used to optimize the thermal distribution of the cells. The main distinction in this algorithm is that while placing the cells in the layout we have clubbed together the cells from the subset containing the hottest cell with the cells from the subset containing the coldest cell. The cells from other two subsets having medium range temperatures are clubbed together. Also these cells are arranged in a particular order giving us almost uniform temperature distribution across the chip. It can be used for optimizing the thermal distribution alone. It partitions the set of cell temperatures in four subsets and assigns a particular color to the cells in the subsets depending on their hotness. It then places the cells in the layout as shown in Figure 1.

Algorithm 1
Input: The Temperature matrix
Output: Optimized Temperature matrix such that maximum value of the window (sub-matrix) temperature is minimized.
• Arrange all the n = m*m (assume m to be an even number) cell temperatures in non-decreasing order (T0,T1…….Tn) • Divide them into 4 sets S1,S2,S3,S4 with temperature values say {T0, T1,……….T(n/4-1)}, {Tn/4, Tn/4+1,……….T(n/2-1)}, {Tn/2, Tn/2+1,……….T(3n/4-1)}, {T3n/4, T3n/4+1,……….T(n-1)}, • Assign colors to the cells in the 4 sets as black (B), pink (P), green (G) and red (R) • Mark the top left corner cell of the layout matix as position (0,0) • Starting from position (0,0), place cells from set S1 in an ascending order i.e. starting from T0 in alternate cell positions i.e. (0+2*i, 0+2*j) in the layout matrix • Starting from position (1,1) , place cells from set S2 in a descending order i.e. starting from T(n/2-1) in alternate cell positions i.e. (1+2*i, 1+2*j) in the layout matrix • Starting from position (1,0), place cells from set S3 in a ascending order i.e. starting from Tn/2 in alternate cell positions i.e. (1+2*i, 0+2*j) in the layout matrix • Starting from position (0,1) , place cells from set S4 in a descending order i.e. starting from T(n-1) in alternate cell positions i.e. (0+2*i, 1+2*j) in the layout matrix

Figure 5: Algorithm 1

We have proposed algorithm 2 (Figure 6) for optimizing the thermal distribution of the cells as well as the total interconnect wirelength. In this algorithm we have implemented game theoretic concept. This is an *n*-player cooperative game. We are choosing a subset of players sequentially to play the game. We choose a seed cell having highest connectivity, and select two sets of players forming two teams. One team consists of neighbouring cells of the seed cell and the other team consists of cells strongly connected to the seed cell. The strategies of the players are to exchange their positions so as to reduce the total wirelength without disturbing the temperature distribution significantly. The payoff of the team is the decrease in the total wirelength *L* by exchanging their positions simultaneously. The players in the two teams play a cooperative game and try to maximize the total payoff. The exchange is allowed only when it gives a positive payoff. In this algorithm we have not imposed any restriction on the quantum of allowed deviation *DeltaT* of the maximum window temperature T_{max} from T_{avg}. Instead we have estimated the percentage deviation of the maximum window temperature T_{max} from T_{avg}. This restriction can easily be incorporated before allowing the exchanges.

Algorithm 2
Input: The Temperature matrix, the adjacency matrix
Output: Optimized Temperature matrix such that maximum value of the window (submatrix) temperature is minimized and the total wirelength is minimized

• Assign colors to the n cells and place them as per algorithm 1
• Mark all the cells as UNPLAYED
• Arrange the cells as per their interconnect weight in the descending order and store in a list L
• Initialize the POINTER = 1 to choose the cell with the highest interconnect weight from the list L as a seed cell
• Initialize NUM_OF_CELL_PLAYED = 0
While (NUM__OF_CELL_PLAYED < n-4)
{
• While (the seed cell has PLAYED){
• Increment the POINTER
• Choose the cell with the next highest interconnect weight at a location given by the POINTER as a seed cell
• } End While
• If (POINTER > n) exit the while loop;
• Select the window in which this cell falls
• Choose 3 nearest neighbours from this window as the first 3 players (say player 1,2,3), note that all the three are of different colors
• Choose the 3 UNPLAYED cells that are heavily connected with the seed cell and are of the same color as of the first three players as second set of players (say player 4,5,6)
Estimate the difference DeltaL = total wirelength before exchange - total wirelength after exchanging the positions of the three pairs of cells with same color
If (DeltaL > 0){
• Exchange player 1 with player 4
• Exchange player 2 with player 5
• Exchange player 3 with player 6
• Mark the seed cell and player 4, player 5, player 6 as PLAYED
• Increment NUM_OF_CELL_PLAYED by 4
• Store minimum total wirelength WL and the corresponding matrix
• }
• Else
• Increment the POINTER to choose the next UNPLAYED cell from the list as a seed cell
• End if
• } End while

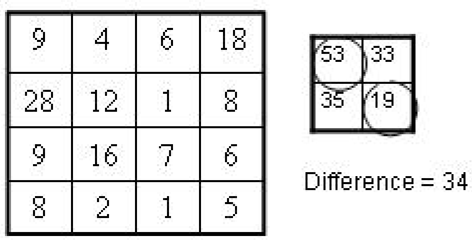
Figure 6: Algorithm 2

Lemma 1: For $t = 2$, each window has four cells with distinct colors.
Proof: We have placed the cells as per algorithm 1 that ensures that each widow has only one cell from a particular temperature band. While exchanging the cells, we are exchanging a cell with only cells of the same color. ■

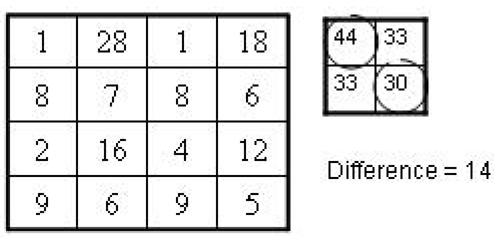
Lemma 2: The algorithm always terminates in finite time.
Proof: The algorithm terminates if all the cells have played or the pointer to select the cell not yet played reduces to zero. Since the pointer is decremented by one after every iteration, the algorithm is guaranteed to terminate after a finite number of iterations. ■

VIII. Illustrations of the Algorithms

The effect of algorithm 1 has been illustrated in Fig. 7. The random cell placement before application of algorithm 1 shows that the maximum difference between the temperatures of windows of size 2X2 is 34. This difference reduces to 14 after application of algorithm 1.



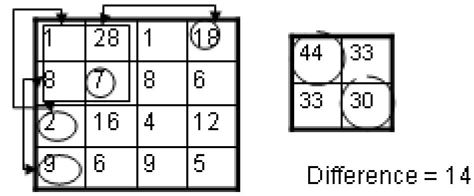
Cell placement before application of algorithm 1



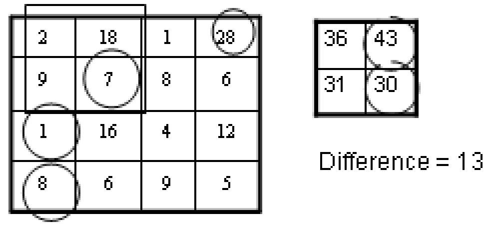
Cell placement after application of algorithm 1

Figure 7: Illustration for Algorithm 1

The effect of algorithm 2 has been illustrated in Fig. 8. The cell placement before application of algorithm 2 shows that the maximum difference between the temperatures of windows of size 2x2 is 14. Algorithm 2 brings the heavily connected cells to the seed cell no 7 and of different colors (i.e. 18, 2 and 9) to the same window as occupied by cell no 7 by exchanging these cells with cell no 28, 1 and 8 respectively. This exchange helps in reducing the total wirelength without affecting the maximum difference in window temperature. In this case we observe that the difference reduces from 14 to 13 after application of algorithm 2.



Cells placement and window temperature before exchange



Cells placement and window temperature after exchange

Figure 8: Illustration for Algorithm 2

IX. Simulation Results and Observations

A. *Comparison of T_{max} achieved*

We have implemented all the algorithms using C and simulated on a computer having AMD Turion64 processor with a clock speed of 1.60 GHz and 512 MB RAM. For the simulation, we have generated random numbers using uniform random distribution representing cell temperatures in the range of 0 to 1000. Similarly the elements of the adjacency matrix for the interconnect weight was generated randomly with weights in the range of 0 to 10. The maximum window temperature T_{max} achieved by both the algorithms have been compared with T_{avg} in Table 1. The percentage deviation from the average window temperature T_{avg} has also been given in the table. As we can see from the histogram in Figure 9 the algorithms reduce the deviation of maximum window temperature from the corresponding T_{avg} value so that the maximum window temperature becomes very close to the ideal average window temperature T_{avg}.

S.No	m	T	Tavg	Tmax (initial)	Tmax (algo1)	Tmax (algo2)	%Deviation (initial)	%Deviation (algo1)	%Deviation (algo2)
1	4	2	1979	3104	2014	2212	56.85	1.77	11.77
2	8	2	1922	2904	2012	2120	51.09	4.68	10.30
3	8	4	7689	8246	7831	7864	7.24	1.85	2.28
4	16	2	1964	3330	1989	2256	69.55	1.27	14.87
5	16	4	7856	9636	7888	8198	22.66	0.41	4.35
6	16	8	31427	32523	31444	31897	3.49	0.05	1.50
7	32	2	1987	3673	2013	2433	84.85	1.31	22.45
8	32	4	7948	9799	8035	8370	23.29	1.09	5.31
9	32	8	31794	33838	32111	33381	6.43	1.00	4.99
10	32	16	127178	129874	128005	128261	2.12	0.65	0.85
11	64	2	1983	3769	1992	2421	90.07	0.45	22.09

Table 1: Comparison of percentage deviation of $\mathbf{T_{max}}$ from $\mathbf{T_{avg}}$ achieved by both the algorithms

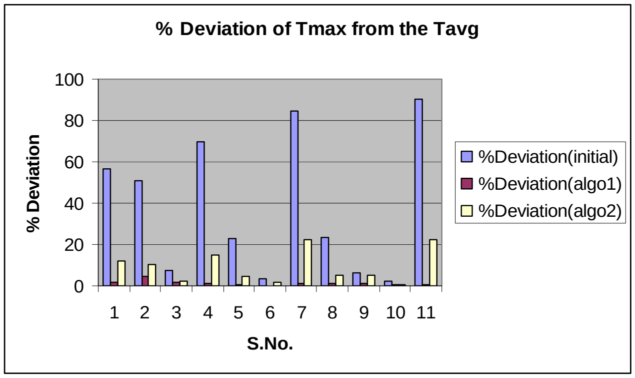


Figure 9: Comparison of deviation (%) of T_{max} from T_{avg}

B. *Comparison of percentage decrease in T_{max} achieved*

The percentage decrease in maximum window temperature T_{max} achieved by both the algorithms have been compared in Table 2. As we can see from the histogram in Figure 10, the percentage decrease in T_{max} achieved by an algorithm normally increases as the problem size (m) increases. We have also noticed that the decrease in T_{max} is largest for a window size 2 and decreases as the window size increases.

S.No	m	T	Tavg	Tmax (initial)	Tmax (algo1)	Tmax (algo2)	%Decrease (algo1)	%Decrease (algo2)
1	4	2	1979	3104	2014	2212	35.12	28.74
2	8	2	1922	2904	2012	2120	30.72	27.00
3	8	4	7689	8246	7831	7864	5.03	4.63
4	16	2	1964	3330	1989	2256	40.27	32.25
5	16	4	7856	9636	7888	8198	18.14	14.92
6	16	8	31427	32523	31444	31897	3.32	1.92
7	32	2	1987	3673	2013	2433	45.19	33.76
8	32	4	7948	9799	8035	8370	18.00	14.58
9	32	8	31794	33838	32111	33381	5.10	1.35
10	32	16	127178	129874	128005	128261	1.44	1.24
11	64	2	1983	3769	1992	2421	47.15	35.77

Table 2: Comparison of percentage decrease in $\mathbf{T_{max}}$ achieved by both the algorithms

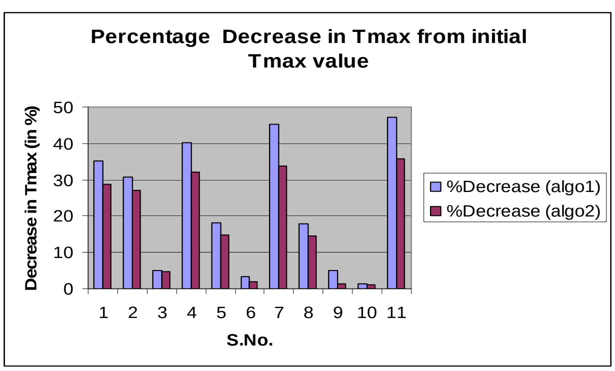


Figure 10: Comparison of decrease (%) in T_{max}

C. *Comparison of percentage decrease in total wirelength (TotalL) achieved*

The percentage decrease in total wirelength (*TotalL*) achieved by both the algorithms have been compared in Table 3. As we can see from the histogram in Figure 11, the percentage decrease in *TotalL* achieved by Algorithm 1 is negative for most of the cases. This implies that the wirelength actually increases. This is expected in Algorithm 1, as it does not consider wirelength while optimizing the temperature distribution. Algorithm 2, on the other hand, attempts to optimize both the total wirelength and the temperature distribution. The percentage decrease in *TotalL* achieved by algorithm 2 normally decreases as the problem size (m) increases. We have also noticed that the decrease in *TotalL* is largest for a window size 2 and decreases as the window size increases.

S.No	m	t	TotalL(0)	TotalL(algo1)	TotalL(algo2)	%dec(algo1)	%dec(algo2)
1	4	2	2978	2810	2674	5.64	10.21
2	8	2	96488	97846	94410	-1.41	2.15
3	8	4	96488	97846	94990	-1.41	1.55
4	16	2	3124248	3133922	3093682	-0.31	0.98
5	16	4	3124248	3133922	3102026	-0.31	0.71
6	16	8	3124248	3133922	3107378	-0.31	0.54
7	32	2	100463960	100524920	99871216	-0.06	0.59
8	32	4	100463960	100524920	99982448	-0.06	0.48
9	32	8	100463960	100524920	100034912	-0.06	0.43
10	32	16	100463960	100524920	100203400	-0.06	0.26
11	64	2	3221448192	3220949504	3211074304	0.02	0.32

Table 3: Comparison of percentage decrease in wirelength achieved by both the algorithms

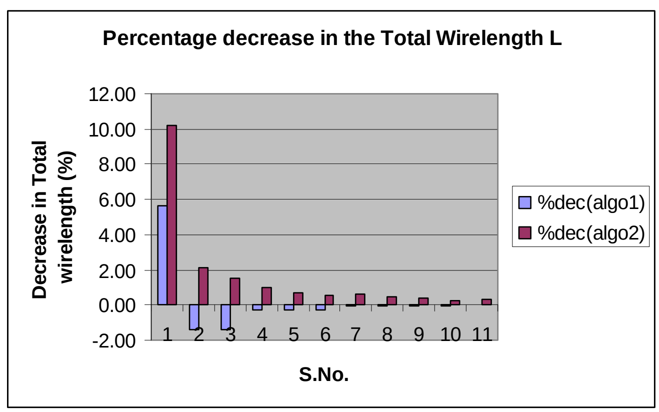


Figure 11: Comparison of decrease (%) in wirelength

D. *Comparison of the CPU times of algorithms*

The empirical values of CPU times (in seconds) of both the algorithms obtained from simulation have been compared in Table 4. As we can see from the histogram in Figure 12, algorithm 1 is very fast but it does not optimize the total wirelength. The CPU times of algorithm 2 normally increases with the problem size i.e. number of cells (m^2). The window size does not seem to have much impact on the CPU times (in seconds) of algorithms.

S.No	m	t	CPU Time taken (algo1)	CPU Time taken (algo2)
1	4	2	0	0.474
2	8	2	0.006	2.101
3	8	4	0.006	2.471
4	16	2	0.019	15.288
5	16	4	0.02	18.73
6	16	8	0.018	19.001
7	32	2	0.03	219.327
8	32	4	0.029	238.99
9	32	8	0.042	232.782
10	32	16	0.042	251.612
11	64	2	0.089	4160.164

Table 4: Comparison of time complexity (in sec) of both the algorithms

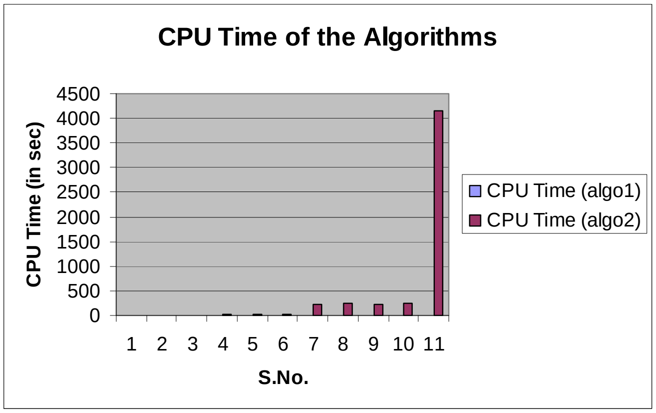


Figure 12: Comparison of CPU time of algorithms

X. CONCLUSION

We have developed a game theoretic formulation to optimize the two objectives of minimizing the maximum temperature of a temperature window and minimizing the total wirelength simultaneously in a multi-objective VLSI design scenario. The algorithms proposed to solve the game have shown potential for being used in optimization tools or EDA tools for chip design industry. Furthermore, the algorithms are generic in nature as the maximum window temperature T_{max} may represent some other parameter such as building density population density etc. in a city and the total wirelength may correspond to the total length of the interconnecting roads. Therefore, they can be modified to plan placement of buildings and roads on a city layout or in the design of retail shop networks for supply chain management. It may also be used for designing pick-up and delivery point networks for logistics and supply chain management. An interesting extension of this work would be to refine the composite payoff function taking into account both the wirelength and the temperature distribution concurrently and generalize the game appropriately.

ACKNOWLEDGEMENTS

We would like to thank Department of Information Technology (DIT), Govt. of India and Indian Institute of Management, Calcutta for providing support for this work.

REFERENCES

[1] S-C Lin, K. Bannerjee and N. Srivastava, Electrothermal engineering in the nanometer era: from devices and interconnects to circuits and systems, Proceedings of the Design Automation Conference, January 2006, pp 223–230.

[2] Sadiq M Sait and Habib Youssef, VLSI Physical Design Automation: Theory and Practice, McGraw Hill Book Company,1995

[3] Chris C. N. Chu and D. F. Wong, A Matrix Synthesis Approach to Thermal Placement, IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems, Vol. 17, NO. 11, November 1998

[4] Narender Hanchate, and Nagarajan Ranganathan, Simultaneous Interconnect Delay and Crosstalk Noise Optimization through Gate Sizing Using Game Theory, IEEE Transactions on Computers, Vol. 55, No. 8, August 2006

[5] Ashok K murugavel and N Ranganathan, A Game-Theoretic Approach for Binding in Behavioural Synthesis, Proc. of the 16th International Conference on VLSI design (VLSI'03), 2003

[6] Avinash Dixit, Susan Skeath, Games of Strategy, 2nd Edition, W.W. Norton & Company, New York, 2004

[7] Ching-Han Tsai and Sung-Mo (Steve) Kang, Cell-Level Placement for Improving Substrate Thermal Distribution, IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems, VOL. 19, No. 2, February 2000